

		Results
14.	((pub-date > 1959 and pub-date < 2002 and FULL-TEXT(test vector) and FULL-TEXT(overlap!)) and sequence) and integrated circuit [All Sources(- All Sciences -)]	14
13.	((pub-date > 1959 and pub-date < 2002 and FULL-TEXT(test vector) and FULL-TEXT(overlap!)) and sequence) and tester [All Sources(- All Sciences -)]	7
12.	(pub-date > 1959 and pub-date < 2002 and FULL-TEXT(test vector) and FULL-TEXT(overlap!)) and sequence [All Sources(- All Sciences -)]	95
11.	pub-date > 1959 and pub-date < 2002 and FULL-TEXT(test vector) and FULL-TEXT(overlap!) [All Sources(- All Sciences -)]	175
10.	(((((pub-date > 1959 and pub-date < 2002 and FULL-TEXT(synchronous) and FULL-TEXT(asynchronous)) and sequence) and state) and clock) and delay) and overlap!) and design) and integrated circuit [All Sources(- All Sciences -)]	19
9.	(((((pub-date > 1959 and pub-date < 2002 and FULL-TEXT(synchronous) and FULL-TEXT(asynchronous)) and sequence) and state) and clock) and delay) and overlap!) and design [All Sources(- All Sciences -)]	129
8.	(((((pub-date > 1959 and pub-date < 2002 and FULL-TEXT(synchronous) and FULL-TEXT(asynchronous)) and sequence) and state) and clock) and delay) and overlap! [All Sources(- All Sciences -)]	147
7.	(((((pub-date > 1959 and pub-date < 2002 and FULL-TEXT(synchronous) and FULL-TEXT(asynchronous)) and sequence) and state) and clock) and delay [All Sources(- All Sciences -)]	503
6.	((((pub-date > 1959 and pub-date < 2002 and FULL-TEXT(synchronous) and FULL-TEXT(asynchronous)) and sequence) and state) and clock [All Sources(- All Sciences -)]	717
5.	((pub-date > 1959 and pub-date < 2002 and FULL-TEXT(synchronous) and FULL-TEXT(asynchronous)) and sequence) and state [All Sources(- All Sciences -)]	2369
4.	(pub-date > 1959 and pub-date < 2002 and FULL-TEXT(synchronous) and FULL-TEXT(asynchronous)) and sequence [All Sources(- All Sciences -)]	3118
3.	pub-date > 1959 and pub-date < 2002 and FULL-TEXT(synchronous) and FULL-TEXT(asynchronous) [All Sources(- All Sciences -)]	6793
2.	pub-date > 1959 and pub-date < 2002 and FULL-TEXT(asynchronous sequence) [All Sources(- All Sciences -)]	13
1.	pub-date > 1959 and pub-date < 2002 and FULL-TEXT(synchronous sequence) [All Sources(- All Sciences -)]	17

Find: [Documents](#)[Citations](#)

Searching for **synchronous and asynchronous and overlap and sequence and state**.

Restrict to: [Header](#) [Title](#) Order by: [Expected citations](#) [Hubs](#) [Usage](#) [Date](#) Try: [Google \(CiteSeer\)](#) [Google \(Web\)](#) [Yahoo!](#) [MSN](#) [CSB](#) [DBLP](#)

5 documents found. **Order: number of citations.**

[Non-Interleaving Semantics for Mobile Processes - Degano, Priami \(1997\) \(Correct\) \(7 citations\)](#)  
of a communication. Also, it can model both a **synchronous**, hand-shake implementation of communications implementation of communications and an **asynchronous** one, typically through a buffer. In the latter In our example, the input of y on link x can **overlap** with or even follow in time the execution of b, [arena.sci.univr.it/~priami/wwwpapers/nis.ps.gz](http://arena.sci.univr.it/~priami/wwwpapers/nis.ps.gz)

**One or more of the query terms is very common - only partial results have been returned. Try [Google \(CiteSeer\)](#).**

[Detecting Global Predicates in Distributed Systems with Clocks - Stoller \(1999\) \(Correct\) \(5 citations\)](#)  
detection, consistent global **states**, partially-**synchronous** systems, distributed debugging, real-time Cooper and Marzullo proposed a solution for **asynchronous** distributed systems [6] Their solution \Phi and that, based on the timestamps, definitely **overlapped** in time. Suppose \Phi actually holds in a [ftp.cs.indiana.edu/pub/stoller/timed-detection.ps.gz](http://ftp.cs.indiana.edu/pub/stoller/timed-detection.ps.gz)

[The verified incremental design of a distributed spanning tree.. - Hesselink \(1997\) \(Correct\) \(2 citations\)](#)  
of concurrency is simpler than the models for **synchronous** communication. 3.1 Invariants An invariant The processes communicate by means of **asynchronous** messages with their neighbours in the graph. and message acceptances of different processes may **overlap**. The possibility and the effect of acceptance, [www.cs.rug.nl/~wim/ghs/whh168.ps](http://www.cs.rug.nl/~wim/ghs/whh168.ps)

[Clustering and Intra-Processor Scheduling for.. - Dixit-Radiya, Panda \(1994\) \(Correct\) \(1 citation\)](#)  
only parallel programs exhibiting logically **synchronous** communication have been addressed. In this shown to be easily applicable even to logically **asynchronous** and irregular task graphs. The goodness of our This model captures communication dependency and **overlap** of communication with computation. This provides [ftp.cis.ohio-state.edu/pub/tech-report/1993/TR11.ps.gz](http://ftp.cis.ohio-state.edu/pub/tech-report/1993/TR11.ps.gz)

[N-ary Speculative Computation of Simulated Annealing on the.. - Andrew Sohn \(Correct\)](#)  
This report presents a practical approach to **synchronous** simulated annealing for massively parallel classified into two categories: **synchronous** and **asynchronous** [4] The **synchronous** approach maintains the of line 1 and line 2. It is therefore difficult to **overlap** or simultaneously execute j-loop iterations. [www.cis.njit.edu/sohn/papers/tpds95.ps.gz](http://www.cis.njit.edu/sohn/papers/tpds95.ps.gz)

Try your query at: [Google \(CiteSeer\)](#) [Google \(Web\)](#) [Yahoo!](#) [MSN](#) [CSB](#) [DBLP](#)

CiteSeer.IST - Copyright [Penn State](#) and [NEC](#)

Find: 

Searching for **synchronous and asynchronous and overlap and sequence and vector**.

Restrict to: [Header](#) [Title](#) Order by: [Expected citations](#) [Hubs](#) [Usage](#) [Date](#) Try: [Google \(CiteSeer\)](#) [Google \(Web\)](#) [Yahoo!](#) [MSN](#) [CSB](#) [DBLP](#)

3 documents found. Order: number of citations.

[On the average near-far resistance for MMSE.. - Upamanyu Madhow.. \(1999\) \(Correct\) \(6 citations\)](#)  
symbol and the filter output. We consider both **synchronous** and **asynchronous** CDMA systems. Although most filter output. We consider both **synchronous** and **asynchronous** CDMA systems. Although most systems in **asynchronous** user, two consecutive bit intervals **overlap** with a given observation interval of length T .  
[tesla.csl.uiuc.edu/~madhow/publications/random.ps](http://tesla.csl.uiuc.edu/~madhow/publications/random.ps)

One or more of the query terms is very common - only partial results have been returned. Try [Google \(CiteSeer\)](#).

[Detecting Global Predicates in Distributed Systems with Clocks - Scott Stoller \(1997\) \(Correct\) \(5 citations\)](#)  
detection, consistent global states, partially-**synchronous** systems, distributed debugging, real-time  
Cooper and Marzullo proposed a solution for **asynchronous** distributed systems [CM91] Their solution  
 $\Phi$  and that, based on the timestamps, definitely **overlapped** in time. Suppose  $\Phi$  actually holds in a  
[ftp.cs.indiana.edu/pub/techreports/TR482.ps](http://ftp.cs.indiana.edu/pub/techreports/TR482.ps)

Try your query at: [Google \(CiteSeer\)](#) [Google \(Web\)](#) [Yahoo!](#) [MSN](#) [CSB](#) [DBLP](#)

CiteSeer.IST - Copyright [Penn State](#) and [NEC](#)

IEEE HOME | SEARCH IEEE | SHOP | WEB ACCOUNT | CONTACT IEEE



Membership Publications/Services Standards Conferences Careers/Jobs

**IEEE Xplore®**  
 RELEASE 1.8

 Welcome  
 United States Patent and Trademark Office

[Help](#) [FAQ](#) [Terms](#) [IEEE Peer Review](#)
[Quick Links](#)
**Welcome to IEEE Xplore®**

- ☐ Home
- ☐ What Can I Access?
- ☐ Log-out

**Tables of Contents**

- ☐ Journals & Magazines
- ☐ Conference Proceedings
- ☐ Standards

**Search**

- ☐ By Author
- ☐ Basic
- ☐ Advanced
- ☐ CrossRef

**Member Services**

- ☐ Join IEEE
- ☐ Establish IEEE Web Account
- ☐ Access the IEEE Member Digital Library

**IEEE Enterprise**

- ☐ Access the IEEE Enterprise File Cabinet

Print Format

**Full-text Search Prototype Results**
[Feedback](#) [Help](#)

 Your search matched **7** of **1043394** documents.

 A maximum of **500** results are displayed, **50** to a page, sorted by **Publication year** in **Descending** order.

**Refine This Search:**

You may refine your search by editing the current search expression or entering a new one in the text box.


☐ Check to search within this result set

**Results Key:**
**JNL** = Journal or Magazine   **CNF** = Conference   **STD** = Standard

**1 Limitations and challenges of computer-aided design technology for CMOS VLSI**
*Bryant, R.E.; Kwang-Ting Cheng; Kahng, A.B.; Keutzer, K.; Maly, W.; Newton, R.; Pileggi, L.; Rabaey, J.M.; Sangiovanni-Vincentelli, A.;*

Proceedings of the IEEE , Volume: 89 , Issue: 3 , March 2001

Pages:341 - 365

[\[Abstract\]](#)   [\[PDF Full-Text \(272 KB\)\]](#)   IEEE JNL

**2 IEEE standard Verilog hardware description language**

IEEE Std 1364-2001 , 2001

Pages:0\_1 - 856

[\[Abstract\]](#)   [\[PDF Full-Text \(3773 KB\)\]](#)   IEEE STD

**3 IEEE standard for VITAL ASIC (application specific integrated circuit) modeling specification**

IEEE Std 1076.4-2000 , 2001

Pages:0\_1 - 420

[\[Abstract\]](#)   [\[PDF Full-Text \(1376 KB\)\]](#)   IEEE STD

**4 Designing asynchronous circuits for low power: an IFIR filter bank for a digital hearing aid**
*Nielsen, L.S.; Sparso, J.;*

Proceedings of the IEEE , Volume: 87 , Issue: 2 , Feb. 1999

Pages:268 - 281

[\[Abstract\]](#)   [\[PDF Full-Text \(492 KB\)\]](#)   IEEE JNL

**5 A design-for-testability technique for register-transfer level circuits using control/data flow extraction**
*Ghosh, I.; Raghunathan, A.; Jha, N.K.;*

Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on , Volume: 17 , Issue: 8 , Aug. 1998

Pages:706 - 723

[\[Abstract\]](#) [\[PDF Full-Text \(360 KB\)\]](#) IEEE JNL

---

**6 IEEE standard for VHDL waveform and vector exchange to support design and test verification (WAVES) language reference manual**

IEEE Std 1029.1-1998 , 28 May 1999

[\[Abstract\]](#) [\[PDF Full-Text \(1020 KB\)\]](#) IEEE STD

---

**7 Logic emulation with virtual wires**

*Babb, J.; Tessier, R.; Dahl, M.; Hanono, S.Z.; Hoki, D.M.; Agarwal, A.;*

Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on , Volume: 16 , Issue: 6 , June 1997

Pages:609 - 626

[\[Abstract\]](#) [\[PDF Full-Text \(520 KB\)\]](#) IEEE JNL

---

[Home](#) | [Log-out](#) | [Journals](#) | [Conference Proceedings](#) | [Standards](#) | [Search by Author](#) | [Basic Search](#) | [Advanced Search](#) | [Join IEEE](#) | [Web Account](#) | [New this week](#) | [OPAC Linking Information](#) | [Your Feedback](#) | [Technical Support](#) | [Email Alerting](#) | [No Robots Please](#) | [Release Notes](#) | [IEEE Online Publications](#) | [Help](#) | [FAQ](#) | [Terms](#) | [Back to Top](#)

Copyright © 2004 IEEE — All rights reserved

IEEE HOME | SEARCH IEEE | SHOP | WEB ACCOUNT | CONTACT IEEE



Membership Publications/Services Standards Conferences Careers/Jobs

**IEEE Xplore®**  
 RELEASE 1.8

 Welcome  
 United States Patent and Trademark Office

[Help](#) [FAQ](#) [Terms](#) [IEEE Peer Review](#)
[Quick Links](#)

## Welcome to IEEE Xplore®

- ☐ Home
- ☐ What Can I Access?
- ☐ Log-out

## Tables of Contents

- ☐ Journals & Magazines
- ☐ Conference Proceedings
- ☐ Standards

## Search

- ☐ By Author
- ☐ Basic
- ☐ Advanced
- ☐ CrossRef

## Member Services

- ☐ Join IEEE
- ☐ Establish IEEE Web Account
- ☐ Access the IEEE Member Digital Library

## IEEE Enterprise

- ☐ Access the IEEE Enterprise File Cabinet

Print Format

## Full-text Search Prototype Results

[Feedback](#) [Help](#)

 Your search matched **16** of **1043394** documents.

 A maximum of **500** results are displayed, **50** to a page, sorted by **Publication year** in **Descending** order.

## Refine This Search:

You may refine your search by editing the current search expression or entering a new one in the text box.


☐ Check to search within this result set

## Results Key:

**JNL** = Journal or Magazine   **CNF** = Conference   **STD** = Standard

## 1 Limitations and challenges of computer-aided design technology for CMOS VLSI

*Bryant, R.E.; Kwang-Ting Cheng; Kahng, A.B.; Keutzer, K.; Maly, W.; Newton, R.; Pileggi, L.; Rabaey, J.M.; Sangiovanni-Vincentelli, A.;*

Proceedings of the IEEE , Volume: 89 , Issue: 3 , March 2001

Pages:341 - 365

[\[Abstract\]](#)   [\[PDF Full-Text \(272 KB\)\]](#)   IEEE JNL

## 2 IEEE standard Verilog hardware description language

IEEE Std 1364-2001 , 2001

Pages:0\_1 - 856

[\[Abstract\]](#)   [\[PDF Full-Text \(3773 KB\)\]](#)   IEEE STD

## 3 IEEE standard for VITAL ASIC (application specific integrated circuit) modeling specification

IEEE Std 1076.4-2000 , 2001

Pages:0\_1 - 420

[\[Abstract\]](#)   [\[PDF Full-Text \(1376 KB\)\]](#)   IEEE STD

## 4 Procedures for static compaction of test sequences for synchronous sequential circuits

*Pomeranz, I.; Reddy, S.M.;*

Computers, IEEE Transactions on , Volume: 49 , Issue: 6 , June 2000

Pages:596 - 607

[\[Abstract\]](#)   [\[PDF Full-Text \(356 KB\)\]](#)   IEEE JNL

## 5 Designing asynchronous circuits for low power: an IFIR filter bank for a digital hearing aid

*Nielsen, L.S.; Sparso, J.;*

Proceedings of the IEEE , Volume: 87 , Issue: 2 , Feb. 1999

Pages:268 - 281

[\[Abstract\]](#)   [\[PDF Full-Text \(492 KB\)\]](#)   IEEE JNL

**6 Static test compaction for synchronous sequential circuits based on vector restoration***Pomeranz, I.; Reddy, S.M.; Guo, R.;*

Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on , Volume: 18 , Issue: 7 , July 1999

Pages:1040 - 1049

[\[Abstract\]](#) [\[PDF Full-Text \(248 KB\)\]](#) IEEE JNL**7 Combining multiple DFT schemes with test generation***Mathew, B.; Saab, D.G.;*

Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on , Volume: 18 , Issue: 6 , June 1999

Pages:685 - 696

[\[Abstract\]](#) [\[PDF Full-Text \(192 KB\)\]](#) IEEE JNL**8 Integration of hierarchical test generation with behavioral synthesis of controller and data path circuits***Bhatia, S.; Jha, N.K.;*

Very Large Scale Integration (VLSI) Systems, IEEE Transactions on , Volume: 6 , Issue: 4 , Dec. 1998

Pages:608 - 619

[\[Abstract\]](#) [\[PDF Full-Text \(240 KB\)\]](#) IEEE JNL**9 A design-for-testability technique for register-transfer level circuits using control/data flow extraction***Ghosh, I.; Raghunathan, A.; Jha, N.K.;*

Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on , Volume: 17 , Issue: 8 , Aug. 1998

Pages:706 - 723

[\[Abstract\]](#) [\[PDF Full-Text \(360 KB\)\]](#) IEEE JNL**10 Test sequences to achieve high defect coverage for synchronous sequential circuits***Pomeranz, I.; Reddy, S.M.;*

Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on , Volume: 17 , Issue: 10 , Oct. 1998

Pages:1017 - 1029

[\[Abstract\]](#) [\[PDF Full-Text \(400 KB\)\]](#) IEEE JNL**11 IEEE standard for VHDL waveform and vector exchange to support design and test verification (WAVES) language reference manual**

IEEE Std 1029.1-1998 , 28 May 1999

[\[Abstract\]](#) [\[PDF Full-Text \(1020 KB\)\]](#) IEEE STD**12 Scheduling tests for VLSI systems under power constraints***Chou, R.M.; Saluja, K.K.; Agrawal, V.D.;*

Very Large Scale Integration (VLSI) Systems, IEEE Transactions on , Volume: 5 , Issue: 2 , June 1997

Pages:175 - 185

[\[Abstract\]](#) [\[PDF Full-Text \(272 KB\)\]](#) IEEE JNL**13 A genetic algorithm framework for test generation***Rudnick, E.M.; Patel, J.H.; Greenstein, G.S.; Niermann, T.M.;*

Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on , Volume: 16 , Issue: 9 , Sept. 1997

Pages:1034 - 1044

[\[Abstract\]](#) [\[PDF Full-Text \(232 KB\)\]](#) IEEE JNL**14 Logic emulation with virtual wires***Babb, J.; Tessier, R.; Dahl, M.; Hanono, S.Z.; Hoki, D.M.; Agarwal, A.;*

Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on , Volume: 16 , Issue: 6 , June 1997

Pages:609 - 626

[\[Abstract\]](#) [\[PDF Full-Text \(520 KB\)\]](#) IEEE JNL

---

**15 Joint maximum-likelihood parameter estimation for burst DS spread-spectrum transmission**

*Rezeanu, S.-C.; Ziemer, R.E.; Wickert, M.A.;*

Communications, IEEE Transactions on , Volume: 45 , Issue: 2 , Feb. 1997

Pages:227 - 238

[\[Abstract\]](#) [\[PDF Full-Text \(452 KB\)\]](#) IEEE JNL

---

**16 CRISP: a pipelined 32-bit microprocessor with 13-kbit of cache memory**

*Berenbaum, A.D.; Colbry, B.W.; Ditzel, D.R.; Freeman, R.D.; McLellan, H.R.; O'Connor, K.J.; Shoji, M.;*

Solid-State Circuits, IEEE Journal of , Volume: 22 , Issue: 5 , Oct 1987

Pages:776 - 782

[\[Abstract\]](#) [\[PDF Full-Text \(1288 KB\)\]](#) IEEE JNL

---

[Home](#) | [Log-out](#) | [Journals](#) | [Conference Proceedings](#) | [Standards](#) | [Search by Author](#) | [Basic Search](#) | [Advanced Search](#) | [Join IEEE](#) | [Web Account](#) | [New this week](#) | [OPAC Linking Information](#) | [Your Feedback](#) | [Technical Support](#) | [Email Alerting](#) | [No Robots Please](#) | [Release Notes](#) | [IEEE Online Publications](#) | [Help](#) | [FAQ](#) | [Terms](#) | [Back to Top](#)

Copyright © 2004 IEEE — All rights reserved




[Subscribe \(Full Service\)](#) [Register \(Limited Service, Free\)](#) [Login](#)

 Search: ☒ The ACM Digital Library ☐ The Guide



## THE ACM DIGITAL LIBRARY


[Feedback](#) [Report a problem](#) [Satisfaction survey](#)

 Published before January 2002  
 Terms used **synchronous sequence**

Found 6 of 119,410

 Sort results by 


 Try an [Advanced Search](#)  
 Try this search in [The ACM Guide](#)

 Display results 

☐ Open results in a new window

Results 1 - 6 of 6

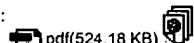
 Relevance scale ☐ ☐ ☐ ☐ ☐

### 1 [Gate delay fault test generation for non-scan circuits](#)

G. Van Brakel, U. Glaser, H. G. Kerkhoff, H. T. Vierhaus

March 1995 **Proceedings of the 1995 European conference on Design and Test**

Full text available:

Additional Information: [full citation](#), [abstract](#)
[Publisher Site](#)

### 2 [Gate-level test generation for sequential circuits](#)

Kwang-Ting Cheng

October 1996 **ACM Transactions on Design Automation of Electronic Systems (TODAES)**, Volume 1 Issue 4

Full text available: pdf(448.19 KB)

Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

### 3 [Processes in a functional animation system](#)

Kavi Arya

November 1989 **Proceedings of the fourth international conference on Functional programming languages and computer architecture**

Full text available: pdf(1.36 MB)

Additional Information: [full citation](#), [references](#), [index terms](#)

### 4 [Convergence rate and termination of asynchronous iterative algorithms](#)

Dimitri P. Bertsekas, John N. Tsitsiklis

June 1986 **Proceedings of the 3rd international conference on Supercomputing**

Full text available: pdf(1.26 MB)

Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

### 5 [Design of heterogeneous ICs for mobile and personal communication systems](#)

Gert Goossens, Ivo Bolsens, Bill Lin, Francky Catthoor

November 1994 **Proceedings of the 1994 IEEE/ACM international conference on Computer-aided design**

Full text available: pdf(1.04 MB)

Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

### 6 [Recurrence equations and the optimization of synchronous logic circuits](#)

M. Damiani, G. De Micheli

July 1992 **Proceedings of the 29th ACM/IEEE conference on Design automation**

Full text available: pdf(630.85 KB)

Additional Information: [full citation](#), [references](#), [citations](#), [index terms](#)

Results 1 - 6 of 6

The ACM Portal is published by the Association for Computing Machinery. Copyright © 2005 ACM, Inc.

[Terms of Usage](#) [Privacy Policy](#) [Code of Ethics](#) [Contact Us](#)

 Useful downloads: [Adobe Acrobat](#) [QuickTime](#) [Windows Media Player](#) [Real Player](#)


[Subscribe \(Full Service\)](#) [Register \(Limited Service, Free\)](#) [Login](#)

Search: The ACM Digital Library The Guide



THE ACM DIGITAL LIBRARY


[Feedback](#) [Report a problem](#) [Satisfaction survey](#)

 Published before January 2002  
 Terms used **asynchronous sequence**

Found 2 of 119,410

 Sort results by 
[Save results to a Binder](#)
[Try an Advanced Search](#)  
[Try this search in The ACM Guide](#)

 Display results 
[Search Tips](#)
☐ [Open results in a new window](#)

Results 1 - 2 of 2

 Relevance scale ☐ ☐ ☐ ☐ ☐

# 1 [Something old: the Gamma 60 the computer that was ahead of its time](#)

M. Bataille

 April 1972 **ACM SIGARCH Computer Architecture News**, Volume 1 Issue 2

 Full text available: [pdf\(511.92 KB\)](#)

 Additional Information: [full citation](#), [references](#)

# 2 [Simulation education: Learning environments for simulation education: design principles for teaching simulation with explorative learning environments](#)

Heimo H. Adelsberger, Markus Bick, Jan M. Pawlowski

 December 2000 **Proceedings of the 32nd conference on Winter simulation**

 Full text available: [pdf\(3.34 MB\)](#)

 Additional Information: [full citation](#), [abstract](#), [references](#)

Results 1 - 2 of 2

The ACM Portal is published by the Association for Computing Machinery. Copyright © 2005 ACM, Inc.

[Terms of Usage](#) [Privacy Policy](#) [Code of Ethics](#) [Contact Us](#)

 Useful downloads: [Adobe Acrobat](#) [QuickTime](#) [Windows Media Player](#) [Real Player](#)